Application of the Two-Way Balanced Amplifier Concept to Wide-Band Power Amplification Using GaAs MESFET's

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Abstract—**An *X*-band GaAs FET power amplifier has been developed, significantly extending the bandwidth capabilities of such amplifiers reported to date. An output power of 1 W with an associated gain of 7.7 dB was achieved from 7.25 to 12.0 GHz by means of combining the power of two amplifier modules. Each of these modules consists of two balanced submodules cascaded to a two-stage unit. The transistor used in the "two-way balanced amplifier" has gate dimensions of 1000×1 μm. The technology, RF performance, and characterization of the transistor are discussed in detail, as are the design and performance of both the single-ended and two-way balanced amplifier modules.**

I. Introduction

BROAD-BAND power amplification with GaAs MESFET's between 4 GHz and 12 GHz was first reported in 1976 with power levels of about 21 dBm in the *C*/*X*-band and 22 dBm in the *C*-band [1]–[3]. In the following years great emphasis was placed into the design of GaAs FET's with higher power at higher frequencies [4]. When these devices became available, they immediately found their way into amplifiers of relatively narrow bandwidth. Power levels in excess of 1 W over bandwidths of almost 15 percent in the *X*-band obtained with a single GaAs FET of 2.4-mm gate width were reported in 1978 [5]. Subsequently, results on a 1-W 2–8-GHz and a 400-mW 11–18-GHz amplifier have been published [6], [7]. The highest power level in the *X*-band reported to date is 39 dBm from 7.7 to 9.9 GHz, accomplished by combining the power of 12 single-ended amplifier modules over this 24 percent bandwidth [8].

This paper describes the design and performance of an amplifier module that combines the output of two submodules to simultaneously achieve high output power and wide bandwidth. Each of the submodules consists of two balanced stages cascaded for better gain performance and phase matched for optimum power and gain performance. The same type of GaAs MESFET is employed in each of the four balanced units. The technology, performance, and modeling of the transistor are discussed in detail. Small-signal design of the matching networks of both the single-ended unit and the "two-way balanced amplifier" is described, as are details of amplifier fabrication and large-signal tuning. Various RF voltages within the transistor under small-signal drive conditions have been calculated. In addition, the RF drain current and the real and the imaginary component of the GaAs FET's output power have been determined. The relationship between these quantities and the reduction in bandwidth that the amplifier experiences when entering nonlinear operation are discussed. The final section describes the performance of the two-way balanced amplifier.

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II. Device Technology and Performance

A. Technology

The GaAs MESFET used in this study, a medium-power device with a total gate width of 1.0 mm, is shown in Fig. 1. Each device has eight 125-μm gate fingers and consists of two subcells. The overall chip size is 370 μm by 800 μm. The 1.0-μm-long gate is centered in a 3.0-μm source–drain channel. In a previous paper [9] we described a GaAs FET with a total gate width of 0.3 mm which was capable of 200 mW of output power up to 18 GHz. The device described here is a wider version of our earlier MESFET, designed for higher output power. The added gate width, and correspondingly larger I_{DSS}, permits this increased output power with somewhat of a penalty in the high frequency performance and ease of matching. The n-type active layers for this MESFET were grown by liquid-phase epitaxy (LPE) on Cr-doped semi-insulating substrates. The epitaxial layer was doped with Sn to a concentration of 1.0×10^{17} cm^{-3} with a thickness of about 0.3 μm. Drift mobility measured using a long-gate FET was found to be within 5 percent of the ideal value for bulk material throughout the thickness of the active layer (4400 cm^2/V·s, 300 K); this is attributed to the incorporation of a substrate etchback prior to growth.

The MESFET channel regions were formed by a self-aligned etched aluminum gate process, the details of which were described earlier [9]. This technique permits high yields and excellent uniformity by allowing for the accurate placement of the gate in the channel across large wafers without a critical alignment. Ohmic contacts were alloyed Au-Ge with a thick Ti-Pt-Au overlay for bonding. The same overlay was also deposited on the gate pad, which was connected to the aluminum gate with a Ti-Pt interconnect metallization. This connection has been

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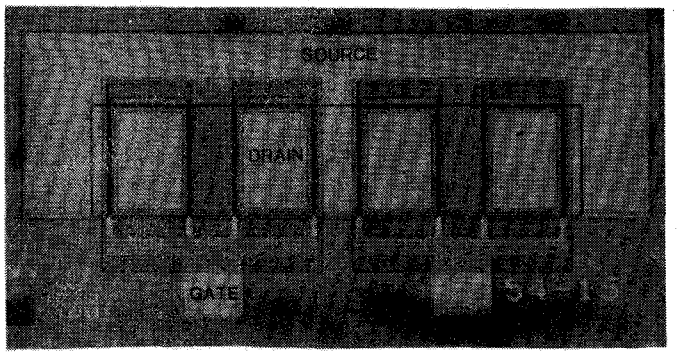


Fig. 1. GaAs MESFET chip, 370×800 μm.

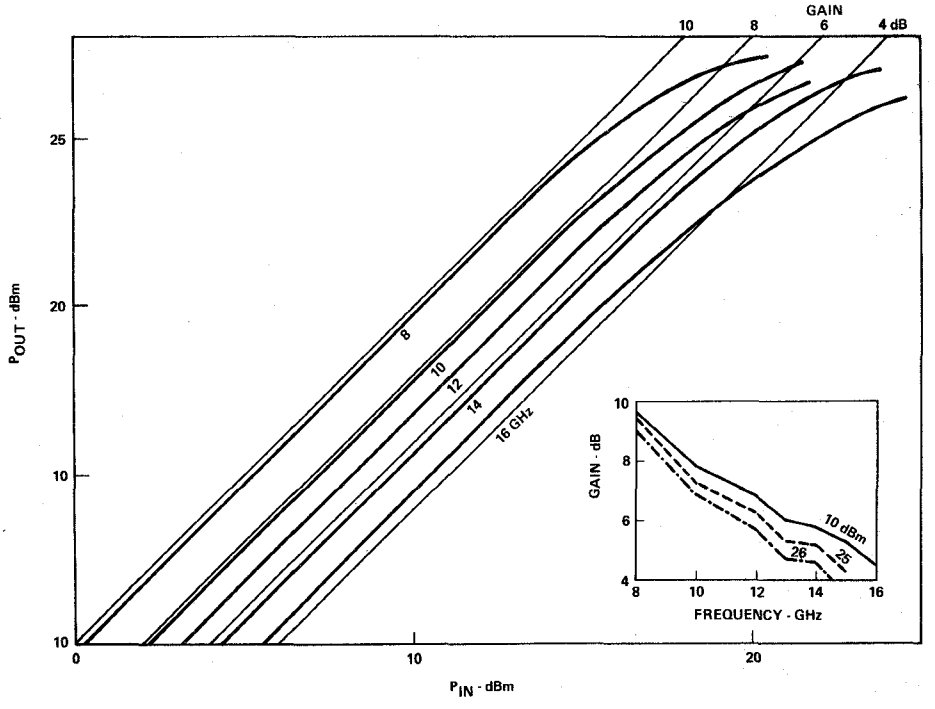


Fig. 2. Transfer curves of the GaAs MESFET at $V_{DS}=9$ V, $V_{GS}=-2.3$ V, and $I_{DS}\simeq 127$ mA.

tested and found to be free of any Au-Al intermetallic phase formation to temperatures as high as 250°C for several thousand hours. As a final processing step, the active region and all aluminum in the device were glassivated.

B. Transistor Performance

The devices used in this study had a saturated drain source current I_{DSS} of 300–400 mA, gate–source pinchoff voltage V_p (for $I_{DS}=0.1$ mA) of 6–8 V and dc transconductance g_{m0} of 65–70 mmho. Drain–source bias voltage was between 8 and 9 V, with gate–source voltage adjusted to give $I_{DS}\approx 0.5\ I_{DSS}$. The transfer curves of the transistor are plotted in Fig. 2 for frequencies between 8 GHz and 16 GHz. Also shown is the frequency dependence of the gain at different output power levels. Power added efficiencies ranged from 31 percent at 8 GHz to 25 percent at 14 GHz for an output power of 26 dBm. At 8 GHz and 27 dBm of output, a power added efficiency of 39 percent was achieved. Small-signal device S-parameters were measured with the aid of an automatic network analyzer, and are shown in Fig. 3.

C. Device Model

The device model that was chosen for the study of various electrical quantities within the device is shown in Fig. 4(a) [10], [11]. It was found to be adequate to characterize the electrical behavior of the transistor in the frequency band from 4–16 GHz. The magnitudes of the device model elements were determined by iteratively matching computed and measured S-parameters between 4 and 16 GHz at frequency points spaced 1 GHz apart. The results are shown in Fig. 3 which compares the measured data (solid curves) with that of the model (dashed curves). The values of the individual elements determined by this process are represented in Fig. 4(b).

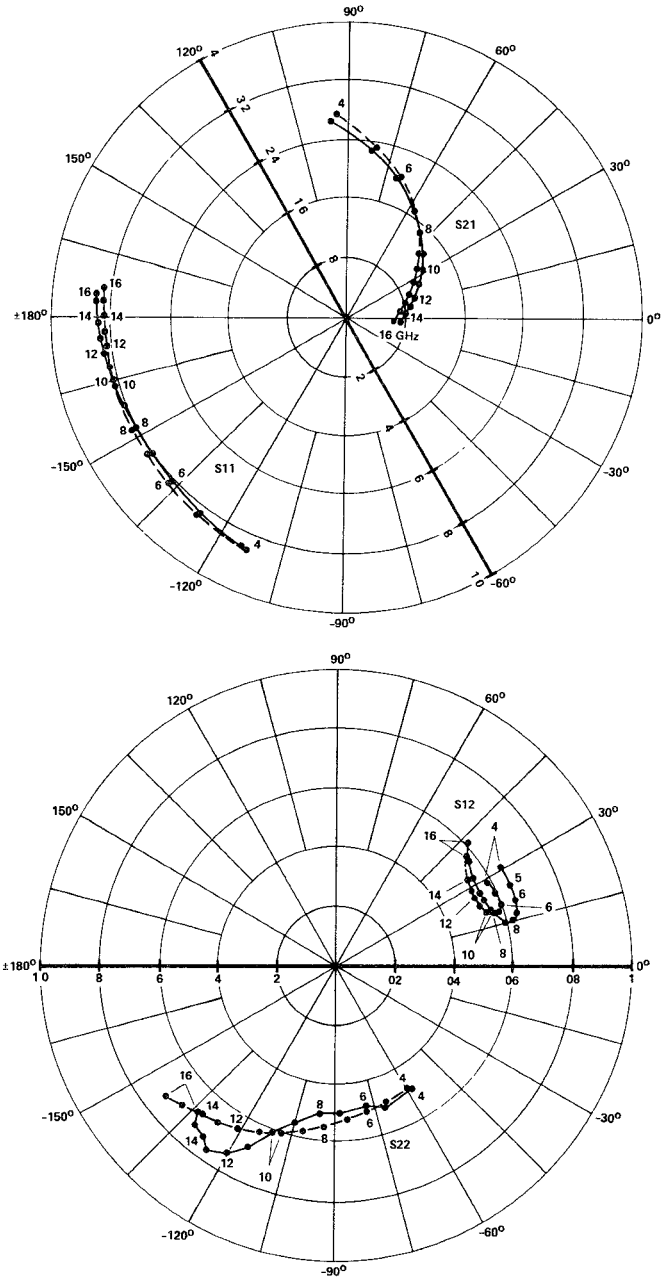


Fig. 3. Comparison of measured (solid curves) S-parameters with values computed for the device model of Fig. 4 (dashed curves).

The good agreement between the measured and computed S-parameters encouraged us to replace the measured data with the model's data in all further computations.

III. Amplifier Design and Performance

A. Small-Signal Design

Based on the experience gained with the design of our 12–18-GHz medium power amplifier modules [7], [9] and with modules in the C-band, the circuit schematic shown in Fig. 5(a) was chosen to provide a flat gain response across the X-band. The transistor model as described in Fig. 4 served as the basis of our design computations. The objective of the input circuit to provide the rejection loss that compensates for the 5-dB/octave gain slope of the

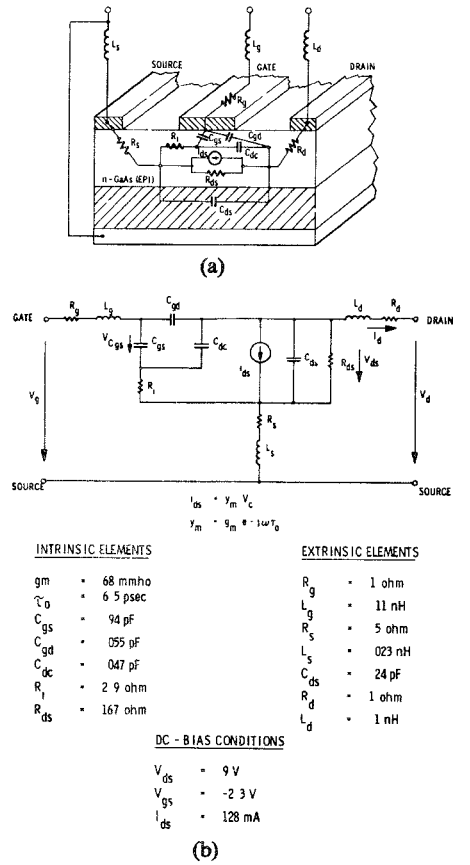


Fig. 4. (a) GaAs MESFET with physical origin of model elements. (b) Schematic of RF equivalent circuit.

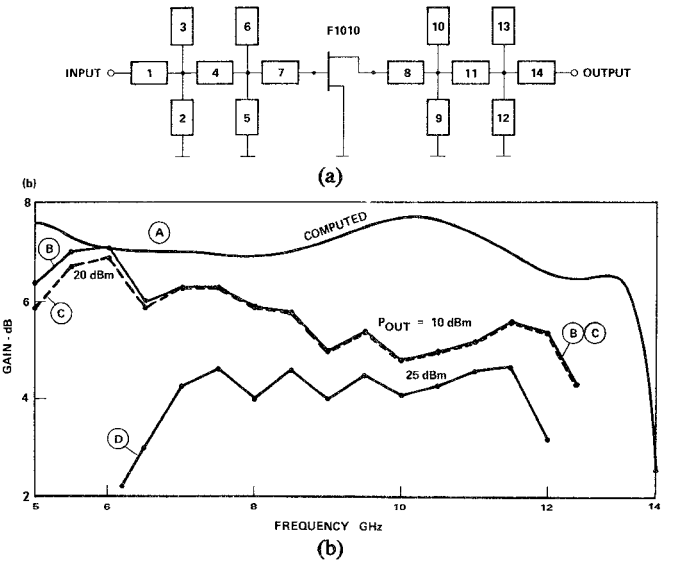
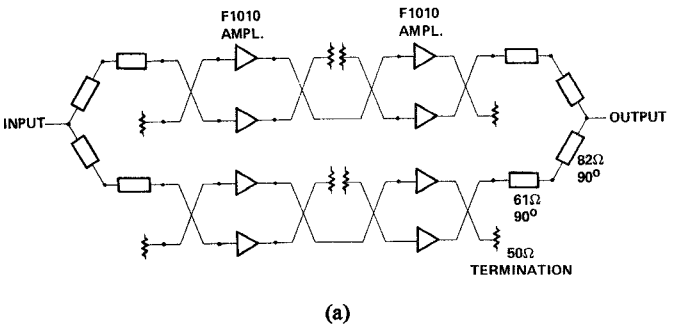


Fig. 5. (a) Schematic of the input and output matching networks. (b) Gain characteristics of the single-ended amplifier module. Curve A: computed using element values listed in Table I. Curve B: measured small-signal gain. Curve D: measured gain at 25-dBm output.

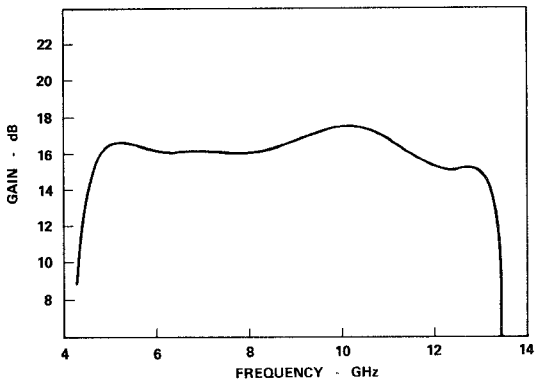
device was met by the circuit elements given in Table I. The design criterion for the output matching network was that of providing the best possible broad-band match in order to maximize output power. The characteristic impedances and electrical lengths of the line elements used in the output circuit are also presented in Table I. They

TABLE I
LINE ELEMENTS OF MATCHING NETWORKS

ELEMENT	IMPEDANCE (Ω)	LENGTH AT 10 GHz
No 1	20 8	75 9°
No 2	58 0	53 3°
No. 3	61 0	63 7°
No 4	50 0	3 4°
No. 5	58 0	51 2°
No. 6	66 0	42 7°
No 7	50 0	4 9°
No. 8	72 0	22.9°
No 9	79 0	29 3°
No 10	91 0	59.7°
No 11	50 0	1 5°
No 12	79 0	29 9°
No 13	91.0	57.6°
No. 14	32 2	86.3°



(a)



(b)

Fig. 6. (a) Circuit diagram of two-way balanced module. (b) Computed small-signal gain using matching networks of Fig. 5(a) and device model of Fig. 4(b).

were determined by means of computer-aided design methods.

The computed small-signal gain response for the amplifier module is presented in curve *A* of Fig. 5(b). The matching networks were assumed to be lossless. Curve *B* of Fig. 5(b) shows the measured small-signal gain for a single-ended module that was tuned for large-signal operation at approximately 20 dBm of input power. A comparison between the computed (*A*) and measured (*B*) small-signal gain in the 7–12-GHz band shows deviations between 1.0 and 2.9 dB. Several factors are responsible for the discrepancy between the computed and the measured gain data. First, the amplifier was tuned for optimum large-signal operation. Second, all of our gain computations did not take into account any circuit losses. Third, the transistors used in the amplifier experiment and the device that was characterized were drawn from several different lots. Curve *C* represents the gain at 25 dBm of output. It reveals that a reduction in bandwidth is experienced when the amplifier module is operated in the large-signal regime. A possible explanation for the large-signal behavior will be presented in Section III-C.

Fig. 6(a) represents the schematic of the two-way balanced module consisting of two pairs of cascaded balanced amplifier stages. Their respective output powers are combined by means of simple two-element power combiners. The computed small-signal-gain performance based on the device model is represented in Fig. 6(b). Due to the reasons given earlier, actual small-signal performance of such a module is expected to trail the computed performance by up to 5 dB when tuned for large-signal operation.

B. MESFET Voltages and Currents and Their Relation to Output Power

The maximum possible drain current of a MESFET ($I_{D\max}$) occurs when the RF-gate voltage equals or exceeds the sum of the gate bias and the Schottky barrier potential. At this point the channel is completely open. The drain current approaches zero when the gate voltage has reached the pinchoff voltage. The maximum instantaneous drain current of a MESFET is therefore limited by the maximum possible dc drain current ($I_{D\max}$), i.e., the peak-to-peak RF drain current cannot exceed $I_{D\max}$. The peak-to-peak voltage at the transistor's output is limited by the drain-to-source breakdown voltage $V_{BDS} = V_{D\max}$ and the minimum drain voltage ($V_{D\min}$) at which the drain current saturation occurs when the gate voltage is zero. This results in a maximum allowable peak RF swing at the drain electrode of $(V_{D\max} - V_{D\min})/2$.

It is well known that the *S*-parameters of a GaAs FET change with input power when approaching saturation. This means that the magnitudes of the elements of the device model change as soon as the device reaches nonlinear operation. Several researchers have modeled GaAs MESFET devices in order to accurately predict the nonlinear microwave performance [12]–[15]. Significant changes in C_{gs}, g_m, C_{gd}, R_i, and R_{ds} were found as a function of both V_{GS} and V_{DS} [12]. As a result, the elements become time dependent as soon as an RF voltage is present that causes nonlinear operation. While voltage and current computations for small-signal operation cannot be applied to a quantitative analysis of the nonlinear characteristics of a MESFET amplifier, they can be used for some qualitative considerations. One such case is the qualitative search for those portions of the frequency band in which nonlinear operation is reached first when the input power to the amplifier is increased.

Using small-signal techniques, we now take a look at the RF voltages on some of the elements of the device model and at the RF drain current. The assumption is made that the device model of Fig. 3 and the magnitudes of its elements represent a physical equivalent for the

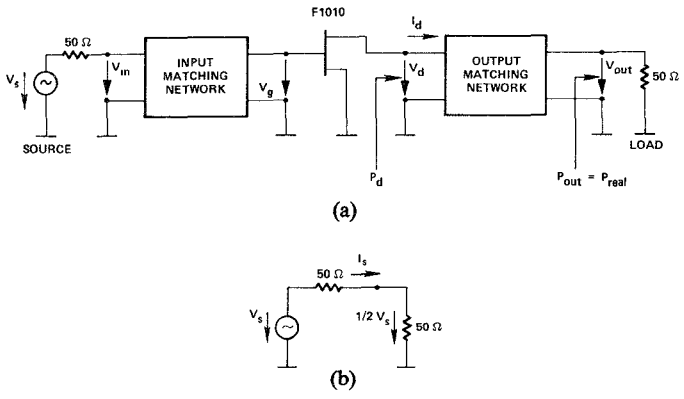


Fig. 7. (a) Block diagram of single-ended amplifier module. (b) Circuit to define reference voltage and current.

transistor. It was briefly discussed in [9] to what extent this assumption can be considered valid.

Fig. 7(a) shows the block diagram of the amplifier module under study. Using this model the voltage on the gate-source capacitance (V_{Cgs}), the voltage across the drain-capacitance (V_{Cds}), the output voltage of the GaAs FET (V_{ds}) and the output voltage of the module (V_{out}) were computed. In addition, we have determined the transistor's RF drain current (I_d). The computed voltages are normalized to $V_s/2$, i.e., that portion of the source voltage (V_s) that appears across a 50-Ω load when the source is terminated into such load. (See Fig. 7(b) for voltage and current normalization.)

The magnitudes and phases of the normalized voltages as they appear on the elements or across the terminals of the transistor are plotted versus frequency in Fig. 8. It is obvious from these plots that the voltage across the drain-source capacitance (V_{Cds}) increases rather rapidly towards the lower end of the frequency band. A similar behavior is shown by the voltage across the gate-source capacitance (V_{Cgs}). Even though all of our computations are in the linear regime, it is safe to conclude that with increasing drive level, nonlinear operation of the amplifier with input power is approached much earlier towards lower frequencies than over the rest of the band. A comparison of curves *B* and *C* in Fig. 5 which show the measured gains of the single-ended amplifier at 10 dBm and 20 dBm of output power supports this conclusion.

A graph of the transistor's normalized drain current (I_d) is presented in Fig. 9. It can be seen that in addition to the sharp increase in RF drain current below 7.5 GHz, an even steeper positive slope exists above 12 GHz. This suggests that saturation due to drain current limitations outside of these two frequencies is approached faster than over the rest of the band.

With the limits for V_d and I_d in mind, it is interesting to determine what portion of the total power $P_d=(V_dI_d^*)/2$ at the MESFET's output terminal represents real or true power and what portion is imaginary power. The power P_d that is available at the drain terminals of the transistor is an apparent power and only part of it will be delivered to the load. The portion of the apparent power that

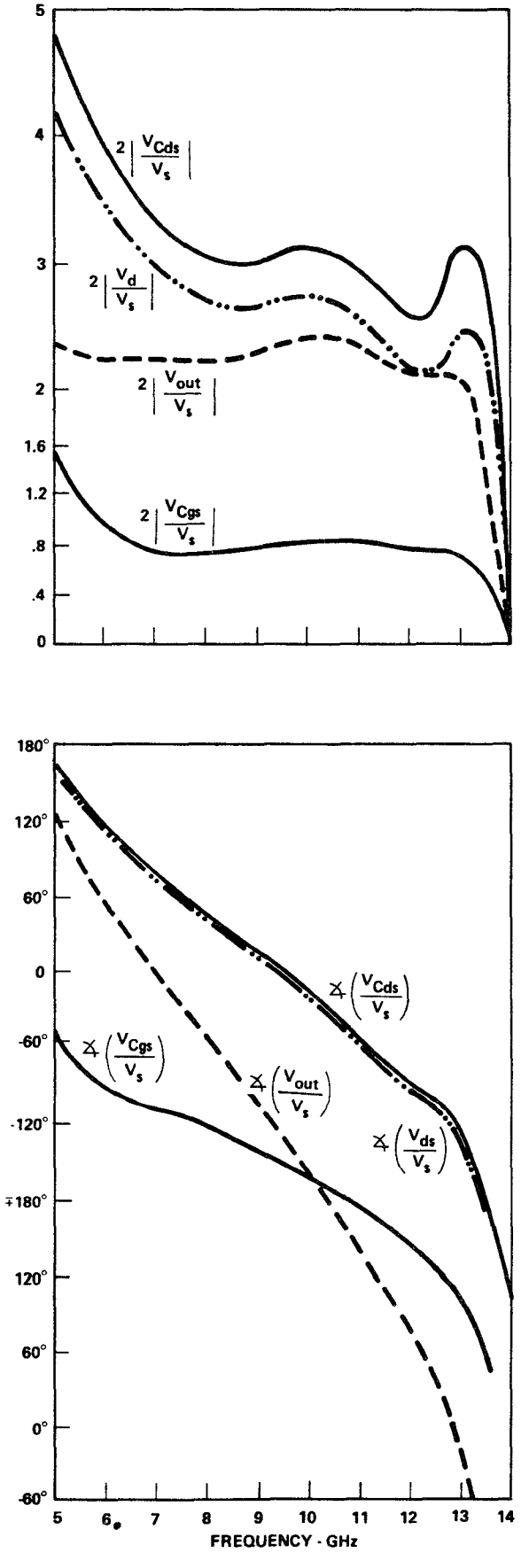


Fig. 8. Normalized RF voltages (magnitude and phase) of GaAs MESFET and amplifier module.

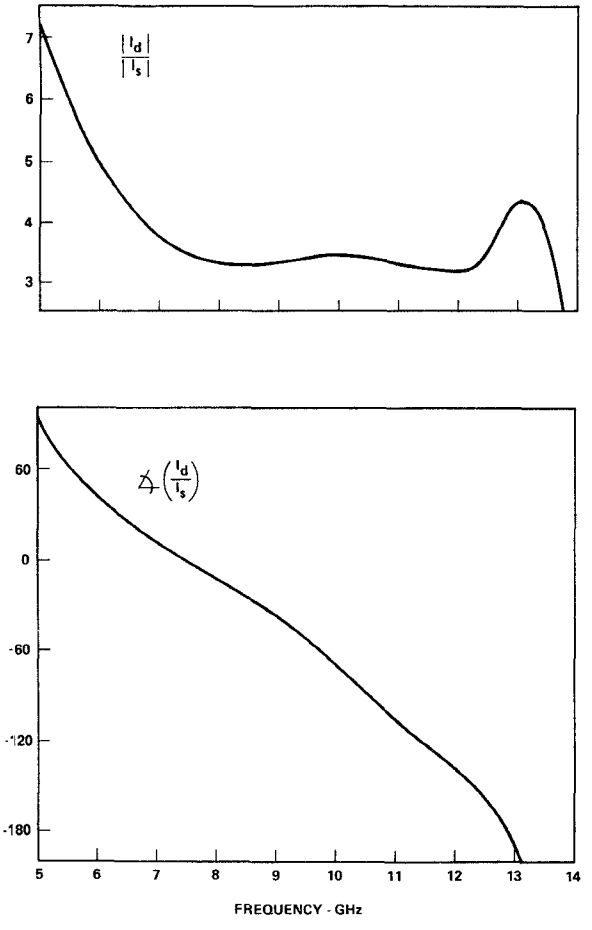


Fig. 9. Normalized RF drain current.

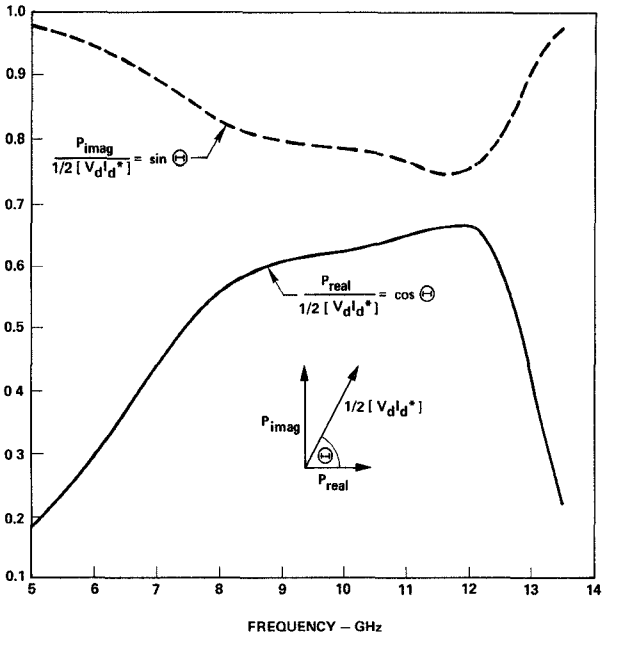


Fig. 10. Power factor of output matching network and normalized imaginary power at drain terminal.

reaches the load, i.e., the true or active power, depends on the qualities of the output matching network and on the reactances of the transistor. The ratio of the true power to the apparent power is known as the power factor. It can be used as a figure of merit for the drain matching network. Since in our study the output matching network is assumed lossless, the real portion of P_d is identical to the power delivered to the load.

The power factor is plotted in Fig. 10 as a function of frequency. Also plotted is the ratio of the imaginary power to apparent power. The curves show that at all frequencies under consideration, the imaginary power exceeds the true power. Since the apparent power is directly related to the voltage and current limitations of the GaAs FET, increasing the output matching circuit's power factor is synonymous with increased output power and efficiency. To accomplish good power matching across a wide frequency band is not an easy task, as is evident from the curve of the power factor. Above 12.5 GHz and below 7.5 GHz the real part of the MESFET's output power falls off rather drastically, suggesting that outside of this frequency range the transistor approaches saturation at a much faster rate than within these limits, i.e., the bandwidth is being reduced due to entering nonlinear operation. This qualitatively agrees with the measurements, as can be seen in Section III-D.

C. *Amplifier Fabrication*

The single-ended input and output circuits of Fig. 5(a) with the line elements of Table I were deposited on 0.015-in thick alumina. The dielectric constant of alumina made it possible to limit the circuit dimensions and thereby the substrate size to a maximum width of 0.300 in per amplifier pair and the overall length of the single-ended module to 0.325 in. With a conducting wall between each pair of single-ended modules, the danger of cavity resonances was prevented. The quadrature couplers and the power combiners were etched into a gold film deposited on 0.015-in thick fused silica. All substrates of the pair of balanced amplifiers were brazed to one molybdenum carrier. The choice of materials for the substrates and the carrier is a compromise between providing an adequate means of heat transfer and a reasonable match of the thermal expansion between the materials involved.

A photograph of the amplifier module is shown in Fig. 11. The input terminal is to the right. In order to achieve the maximum obtainable output power, the two cascaded balanced amplifiers, as well as the individual arms of the combiner/divider networks, must be phase matched to within 20° of each other [7]. This requires careful assembly and identical tuning in both branches of the two-way cascaded amplifier.

D. *Amplifier Performance*

The large-signal gain performance of the single-ended amplifier module that constitutes the basic element of the two-way balanced power amplifier is presented as curve *C* of Fig. 5(b). The gain is plotted as a function of frequency at a constant output power of 25 dBm. The tuning of this single-ended module was performed at an input power

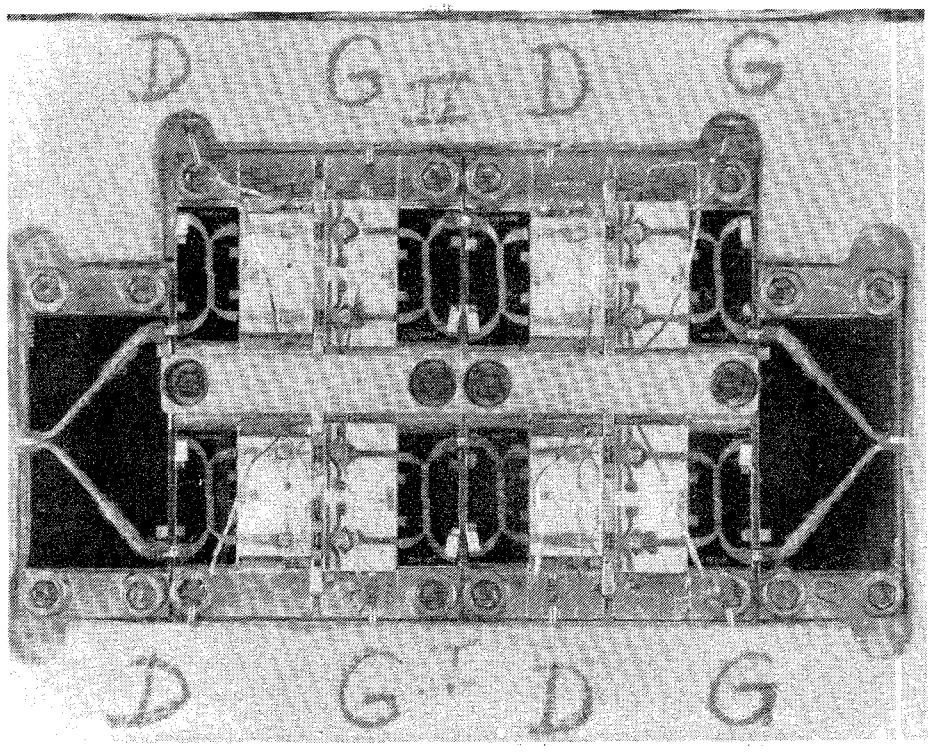


Fig. 11. Photograph of the two-way balanced module.

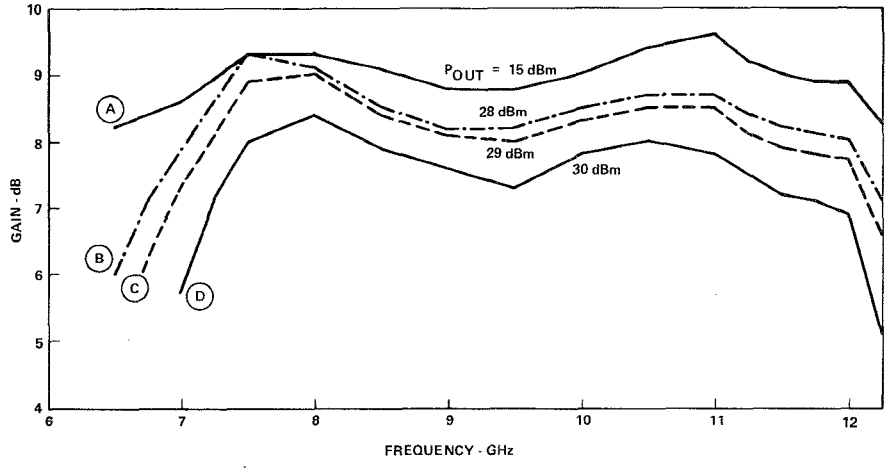


Fig. 12. Gain of two-way balanced module with output power as parameter.

level of approximately 19 dBm. The large-signal tuning process resulted in reduction of the characteristic impedances at the open ends of elements No. 3 and No. 13, as well as a reduction in length of elements No. 1 and No. 14 (see Fig. 5 (a)). In addition, elements No. 1 and No. 14 took on a tapered shape as can be seen in Fig. 11.

Curve *A* of Fig. 12 represents the small-signal gain of the "two-way cascaded balanced amplifier" whose schematic diagram is shown in Fig. 6(a). This performance was measured after the amplifier was tuned for large-signal operation at an input level of approximately 21 dBm. Large-signal tuning of the two-way cascaded balanced amplifier did deviate only slightly from that of the single-ended module whose performance was presented in Fig. 5(b). However, in the process of optimizing the unit's gain performance, the two-way dividers at both ends of the amplifier ended up with the 61-Ω elements being altered to a tapered transmission line.

Curves *B* through *D* represent the gain performance of the amplifier at three levels of output power: 28, 29, and 30 dBm. The performance characteristics of the two-way cascaded balanced amplifier are summarized in Table II. All results presented in Table II and Fig. 12 were obtained after the unit was tuned for large-signal operation. The maximum input and output SWR's of the amplifier between 6.5 and 12.25 GHz were 1.8 and 1.75, respectively.

The gain curves in Fig. 12 show very clearly the band-

TABLE II
LARGE SIGNAL AMPLIFIER PERFORMANCE

FREQUENCY BAND GHz	MINIMUM OUTPUT dBm	GAIN dB	GAIN VARIATION dB	MAXIMUM COMPRESSION dB	RELATIVE BANDWIDTH %
7 - 12 0	27	9.0	±.7	6	52.6
7 - 12.0	28	8 6	± 7	9	52.6
7 - 12.0	29	8.3	± 7	1.3	52.6
7.25 - 12.0	30	7.7	± 75	2.0	49 4

width reduction with increasing output power. It is especially pronounced for frequencies below 7.5 GHz and above 12 GHz, as predicted on the basis of the power factor plot shown in Fig. 10.

IV. CONCLUSION

It has been demonstrated that combining the power of two cascaded balanced amplifiers is a feasible concept for broadband power amplification with GaAs MESFET's. The two-way balanced amplifier offers the advantages that are typical for balanced amplification, such as low return loss and smooth gain response. In addition, it has the benefit of better heat dissipation by subdividing and spreading the sources of heat. The principal benefit, however, is that of bandwidth capability, i.e., narrower gate devices are easier to match over wide bandwidths than the lower impedance wide gate devices.

The design of a 7–12-GHz two-way balanced amplifier using a 1000-μm gate width GaAs MESFET has been described. The 1-μm gate length device was developed with special emphasis placed on amplification capability through the X-band, compromising between power and bandwidth capabilities. Spot frequency measurements of the device at 12 GHz resulted in output powers as high as 450 mW, with 5.3-dB gain and 30-percent power added efficiency. A model of the GaAs MESFET was developed and used in the design of the amplifier. The power factor of the output matching network was determined and, from its dependence on frequency, qualitative conclusions were drawn in regard to bandwidth reduction with increasing input power. An instantaneous output power of 1 W across 7.25–12 GHz was achieved. The attendant gain was 7.7 ± 0.75 dB. These results demonstrate the outstanding broad-band capabilities of the two-way balanced amplifier concept and the excellent broad-band power capabilities of the transistor used at frequencies up to 12 GHz.

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